# ABSTRACT

A time-interleaved bandpass delta-sigma modulator is developed which includes a first adder and a second adder and a comparator. An input signal is transmitted to the first adder according to the clock frequency of each channel block, and an n channel block output $u_n$ of the first adder is transmitted to the first adder and the second adder of an n+2 channel block, and an n block output $v_n$ of the second adder is transmitted to the second adder of an n+2 block, and an output $y_n$ that passes through an n block comparator is transmitted to the first adder and the second adder of an n+2 block. Therefore, a modulator sequentially receives output from the comparator of each block for generating the final output y.

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